**PVP 20**

**Code: 20EE3602**

**III B.Tech - II Semester – Regular / Supplementary Examinations**
**APRIL 2024**

# MICROPROCESSORS AND MICROCONTROLLERS
## (ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

| | | | BL | CO | Max. Marks |
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| **UNIT-I** | | | | | |
| 1 | a) | The Bus Interface Unit and Execution Unit of 8086 microprocessor does the parallel processing of Instructions. Design a flow chart for sequence of steps in execution of instructions. | L2 | CO1 | 6 M |
| | b) | The following are the contents of various Registers of 8086<br>$AX - 3000H$<br>$BX - 2000H$<br>$SI - 3500H$<br>$DI - 3000H$<br>$2000:5500 - 50H$<br>$BP - 5000H$<br>i) MOV CL, [BX + DI + 500H]<br>ii) INC SI<br>iii) MOV [DI + 0700], AH<br>iv) MOV [BP+DI+700], BH.<br>Mention the contents of each register after execution of each instruction. | L3 | CO2 | 8 M |

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| | | **OR** | | | |
| 2 | a) | Instruction queue is fixed with a size of 6 bytes. Using a suitable example state the reason for limiting the size of instruction prefetch queue. | L3 | CO1 | 4 M |
| | b) | Calculate the Physical Address if the Segment Address is 2000H and the Offset address is 1000H. | L3 | CO2 | 4 M |
| | c) | With a neat diagram explain the timing diagram of read operation in maximum mode. | L2 | CO1 | 6 M |
| | | **UNIT-II** | | | |
| 3 | a) | Using all suitable addressing modes write an instruction to transfer a data byte from 24200H memory location to AX Register. | L2 | CO2 | 8 M |
| | b) | Explain in detail the below Assembler directives with examples.<br>i) EQU ii) DW iii) PROC iv) PUBLIC | L3 | CO3 | 6 M |
| | | **OR** | | | |
| 4 | a) | Interpret the result of the following instructions<br>i) XOR AX, AX<br>ii) AND BX, 00FFH<br>iii) CMP AX,BX<br>iv) TEST AL,08H | L3 | CO3 | 7 M |
| | b) | Write a program to transfer 100H bytes are stand in memory location address at 1000:0300H transfer these data bytes to another memory location address starting from 1000:0700H using PUSH & POP instructions. | L3 | CO3 | 7 M |

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| **UNIT-III** | | | | | |
| 5 | a) | Illustrate the list of operations takes place when an interrupt is generated to 8086 through 8259 Programmable Interrupt Controller. | L2 | CO3 | 6 M |
| | b) | Interface an 8257 with 8086 to transfer 2KB of data from memory to I/O device. Assume appropriate address. | L4 | CO4 | 8 M |
| **OR** | | | | | |
| 6 | a) | Illustrate the architecture of 8255 PPI. | L4 | CO4 | 7 M |
| | b) | Draw and explain the pin diagram of 8251 USART. | L3 | CO4 | 7 M |
| **UNIT-IV** | | | | | |
| 7 | a) | Draw the pin diagram of 8051 and explain function of each pin. | L2 | CO2 | 8 M |
| | b) | Explain about the register banks and special function registers of 8051 in detail. | L3 | CO2 | 6 M |
| **OR** | | | | | |
| 8 | a) | Explain the internal and external program memory as well as data memory of 8051 with the diagram showing their capacities. | L3 | CO4 | 7 M |
| | b) | Distinguish between ACALL and LCALL instructions and explain their advantages and disadvantages. | L2 | CO2 | 7 M |
| **UNIT-V** | | | | | |
| 9 | a) | Explain following instructions.<br>i. XCHD A, R1<br>ii. MOVC A,@A+DPTR<br>iii. MOV A, 50H<br>iv. MOV R7,#50H<br>v. MOV 50H ,#50H | L2 | CO3 | 7 M |

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| | b) | Interface an ADC with 8051 and write a program to read an Digital O/P at port2 and store it at the memory location 54H. | L3 | CO4 | 7 M |
| | | **OR** | | | |
| 10 | a) | Analyze the A and B registers after execution of following program.<br>Write the output after the execution of each instruction<br>ORG 00H<br>MOV A,#12H<br>MOV B,#14H<br>DIV AB<br>CLR A<br>CPL ACC.0<br>END | L3 | CO3 | 6 M |
| | b) | Draw and explain interfacing diagram of ADC with 8051 microcontroller. | L4 | CO4 | 8 M |